2 T855 Circuit Operation

This section provides a basic description of the circuit operation of the T855 receiver.

Note: Unless otherwise specified, the term "PGM800Win" used in this and following sections refers to version 2.00 and later of the software.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB. The parts list and diagrams for the VCO PCB are in Part E.

The following topics are covered in this section.

2.1 Introduction

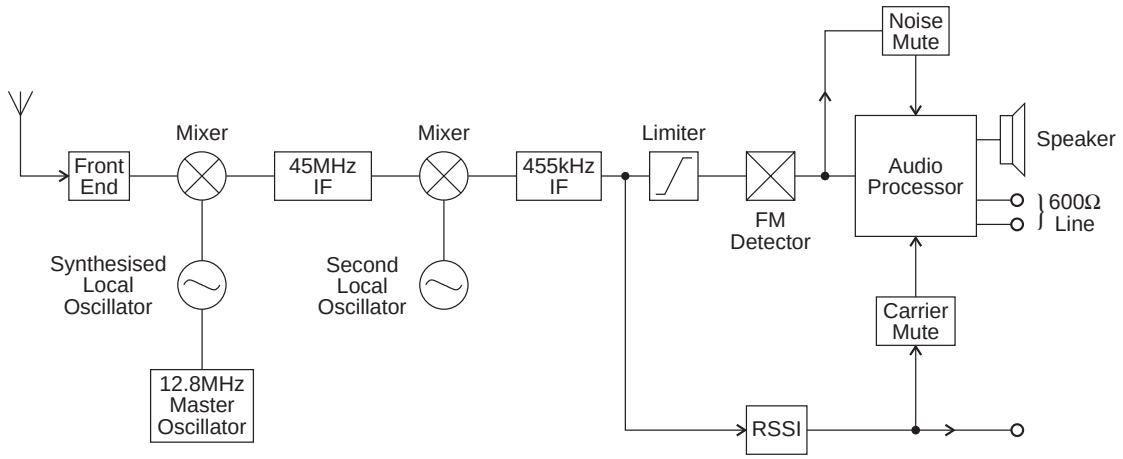

Figure 2.1 T855 High Level Block Diagram

The T855 receiver consists of a number of distinct stages:

- front end
- mixer
- synthesised local oscillator
- IF
- audio processor
- mute (squelch)
- regulator circuits
- received signal strength indicator (RSSI).

These stages are clearly identifiable in Figure 2.1. Refer to the circuit diagrams in Section 6 for further detail.

2.2 Receiver Front End

(Refer to the front end, IF section and audio processor circuit diagrams (sheets 4, 3 and 2 respectively) in Section 6.3.)

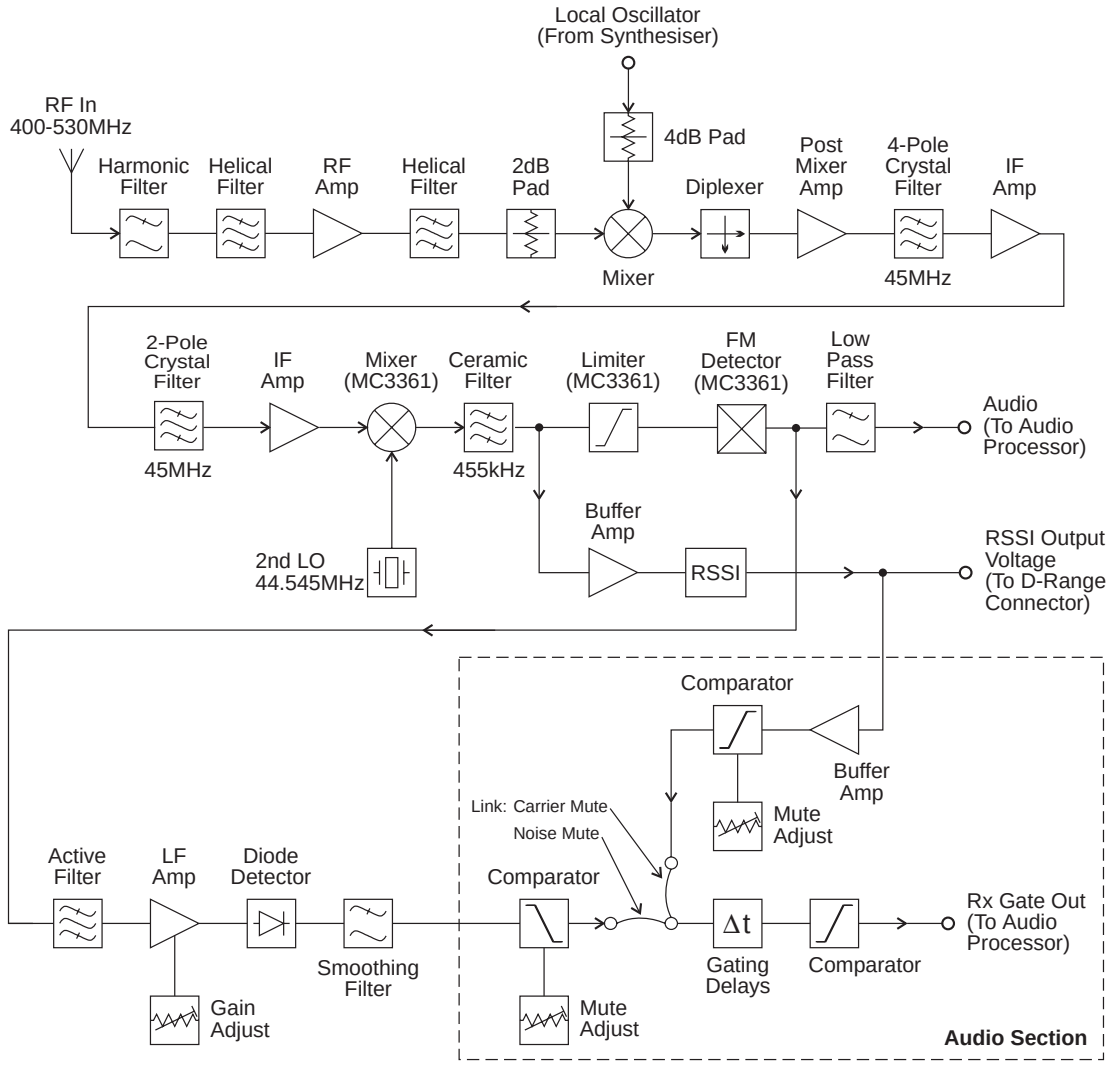

Figure 2.2 T855 Front End, IF and Mute Block Diagram

The incoming signal from the N-type antenna socket is fed through a 9-pole, low pass filter with a cut frequency of approximately 600MHz. This low loss filter (typically less than 0.5dB over 400-530MHz) provides excellent immunity to interference from high frequency signals.

The signal is then further filtered, using a high performance helical resonator doublet (FL410) which provides exceptional image rejection, before being amplified by approximately 8dB (Q410). The signal is then passed through a further helical filter doublet (FL420) before being presented to the mixer via a 2dB attenuator pad.

Each sub-block within the front end has been designed with 50 ohm terminations for ease of testing and fault finding. The overall gain from the antenna socket to the mixer input is approximately 2dB.

2.3 Mixer

(Refer to the front end circuit diagram (sheet 4) in Section 6.3 and Figure 2.2.)

IC410 is a high level mixer requiring a local oscillator (LO) drive level of +17dBm (nominal). The voltage controlled oscillator (VCO) generates a level of +21dBm (typical) and this is fed to the mixer via a 5dB attenuator pad. A diplexer terminates the IF port of the mixer in a good 50 ohms, thus preventing unnecessary intermodulation distortion.

2.4 IF Circuitry

(Refer to the IF section circuit diagram (sheet 3) in Section 6.3 and Figure 2.2.)

Losses in the mixer are made up for in a tuned, common gate, post mixer amplifier (Q310). Several stages of amplification and filtering are employed in the IF circuitry. The first crystal filter is a 4-pole device (&XF300) which is matched into 50 ohms on both its input and output ports. This stage is followed by a common base amplifier (Q320) whose output is matched into a 2-pole crystal filter (&XF301). The signal is then amplified using a high gain MOSFET amplifier (Q330), after which the signal is mixed down to 455kHz with the second crystal local oscillator (44.5455MHz).

The 455kHz signal is filtered using a 6-pole ceramic filter (&XF302) before being limited and detected. Q340 provides a buffered 455kHz output for use with the optional RF level detector (RSSI)

The second IF mixer, limiter and detector is in a 16-pin IC (IC310). Quadrature detection is employed, using L390, and the recovered audio on pin 9 of IC310 is typically 1V p-p for 60% system deviation.

2.5 Noise Mute (Squelch)

(Refer to the audio processor and IF section circuit diagrams (sheets 2 and 3 respectively) in Section 6.3 and Figure 2.2.)

The noise mute operates on the detected noise outside the audio bandwidth. An operational amplifier in IC310 is used as an active band pass filter centred on 70kHz to filter out audio components. The noise spectrum is then further amplified in a variable gain, two-stage amplifier (Q350 & Q360) with additional filtering. The noise is then rectified (D310) and filtered to produce a DC voltage proportional to the noise amplitude. The lowest average DC voltage corresponds to a high RF signal strength and the highest DC voltage corresponds to no signal at the RF input.

The rectified noise voltage is compared with a threshold voltage set up on RV230, the front panel "Gating Sensitivity" potentiometer. Hysteresis is provided by the feedback resistor (R267) to prevent the received message from being chopped when the average noise voltage is close to the threshold. R281 and R280 determine the mute opening and closing times and, in combination with solder links SL210 and SL220, provide three time delay options (SL210 is linked as standard - refer to Section 3.8). The mute control signal at pin 7 of IC270 is used to disable the speaker and line audio outputs. The speaker output can be separately enabled for test purposes by operating the front panel mute disable switch, SW201.

2.6 Carrier Mute

(Refer to the audio processor and IF section circuit diagrams (sheets 2 and 3 respectively) in Section 6.3 and Figure 2.2.)

A high level carrier mute facility is also available. The RSSI (refer to Section 2.12) provides a DC voltage proportional to the signal strength. This voltage is compared with a preset level, set up on RV235, and may be linked into the mute timing circuit using PL250. PL250 selects either the noise mute or the carrier mute. From this point both the noise and carrier mute circuits operate in the same manner, using common circuitry.

2.7 Audio Processor

(Refer to the audio processor circuit diagram (sheet 2) in Section 6.3.)

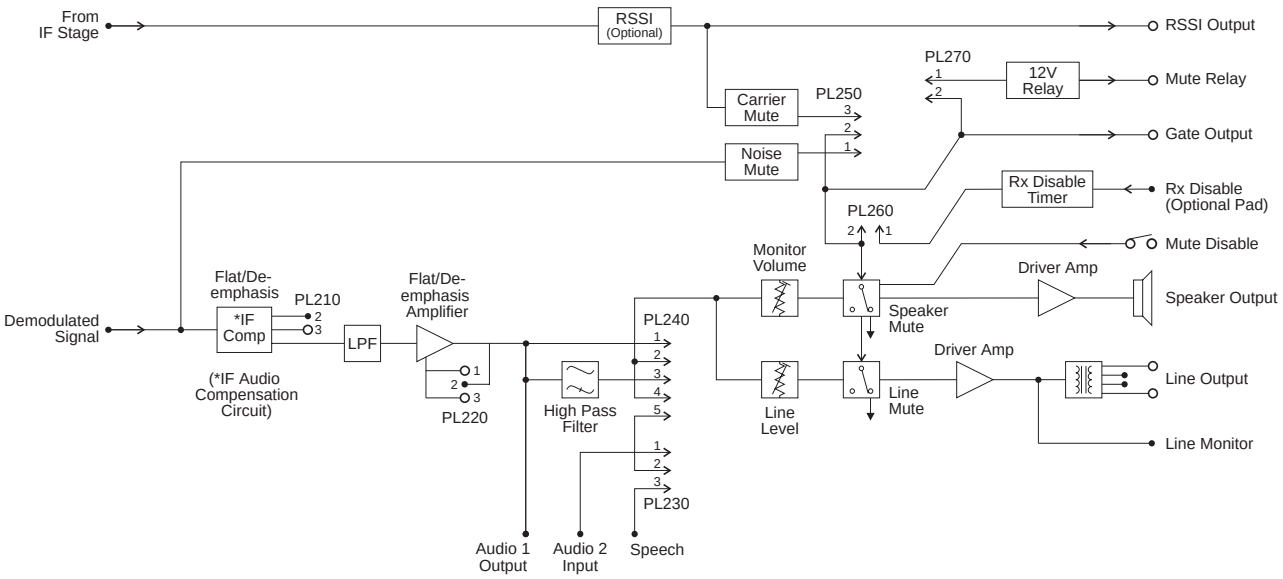

Figure 2.3 T855 Audio Processor Block Diagram

The recovered audio on pin 9 of IC310 is passed through a compensation network and processed in a third order elliptic active filter to give the required response. Linking (PL220 & PL210) is available to give either a flat or de-emphasised audio response, with de-emphasis giving a -6dB/octave roll off. The output of IC210 is split to provide separate paths for the speaker and line outputs. The "Audio 1", Audio 2" and "Speech" lines allow access to the receiver's audio path for external signalling purposes (refer to Section 3.5).

The signals are passed to audio drive amplifiers IC240 and IC260. Under muted conditions the inputs of these amplifiers are shunted to ground via transistors Q230 and Q290 respectively. The audio output of IC240 has a DC component which is removed by C249, and this then drives a speaker directly. The output of IC260 is fed into a line transformer to provide a balanced 2-wire or 4-wire, 600 ohm output.

The speaker volume is set using the front panel "Monitor Volume" knob (RV205) and the line level is set using the recessed "Line Level" potentiometer (RV210).

The red front panel "Gate" LED (D250) indicates the status of the mute circuit. When a signal above the mute threshold is received, the LED is illuminated. The "Monitor Mute" switch (SW201) on the front panel opens the mute, allowing continuous monitoring of the audio signal (on = audio muted; off = audio unmuted).

The mute control line is available on pad 234 ("RX GATE OUT") for control of external circuitry. A high (9V) on pad 234 indicates that the audio is disabled and a low (0V) indicates that a signal above the mute threshold level is being received.

The audio can also be disabled using the "RX-DISABLE" inputs, pads 225 or 228, having connected the "RX-DISABLE" link between pins 1 & 2 of PL260. An adjustable time delay (RV220) is provided on these lines. In order to disable the audio, either pad must be pulled to 0V (refer to Section 1.4 in Part G).

An undedicated relay is provided (RL210) for transmitter keying or other functions and this can be operated from the mute line by linking PL270.

2.8 Power Supply And Regulators

(Refer to the regulators circuit diagram (sheet 6) in Section 6.3.)

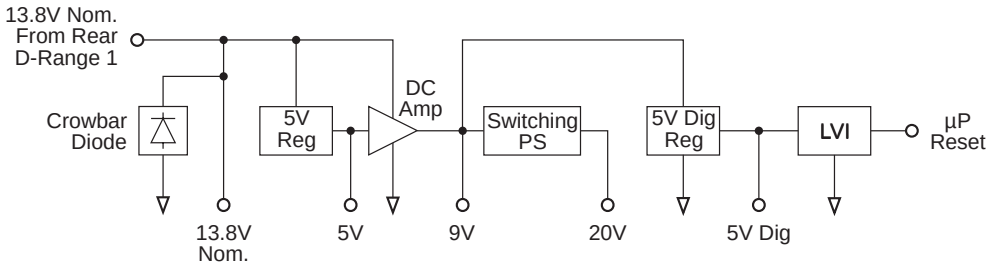

Figure 2.4 T855 Power Supply And Regulators Block Diagram

The T855 is designed to operate off a 10.8-16V DC supply (13.8V nominal). A 5.3V regulator (IC630) runs directly from the 13.8V rail, driving much of the synthesiser circuitry. It is also used as the reference for a DC amplifier (IC640, Q630 & Q620) which provides a medium current capability 9V supply.

A switching power supply, based on Q670 and Q660, runs off the 9V supply and provides a low current capability +20V supply. This is used to drive the synthesiser loop filter (IC740), giving a VCO control voltage of up to 20V.

The 13.8V supply drives both output audio amplifiers without additional regulation. A separate 5V regulator (IC610) drives the microprocessor and associated digital circuitry. The output of this regulator is monitored by the Low Voltage Interrupt (LVI) circuit (IC650).

A crowbar diode is fitted for protection against connection to a power supply of incorrect polarity. It also provides transient overvoltage protection.

Note: A fuse must be fitted in the power supply line for the diode to provide effective protection.

2.9 Microcontroller

(Refer to the microcontroller circuit diagram (sheet 8) in Section 6.3.)

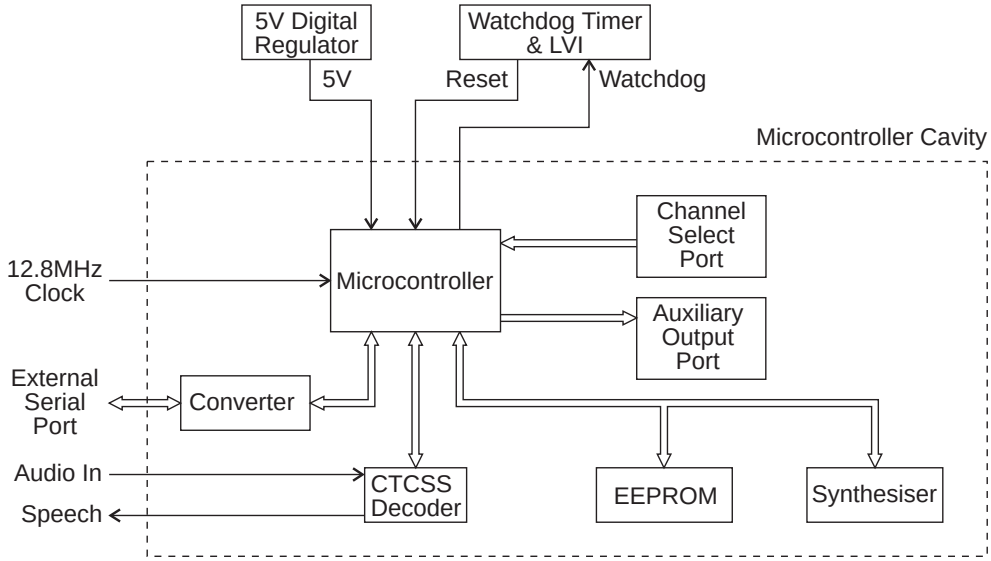

Figure 2.5 T855 Microcontroller Block Diagram

Overall system control of the T855 is accomplished by the use of a member of the 80C51 family of microcontrollers (IC810) which runs from internal ROM and RAM. Four ports are available for input/output functions.

Non-volatile data storage is achieved by serial communication with a 16kBit EEPROM (IC820). This serial bus is also used by the microcontroller to program the synthesiser (IC740).

The main tasks of the microcontroller are as follows:

- program the synthesiser;
- interface with the PGM800Win programming software at 9600 baud via the serial communication lines on D-range 1 (PL100) & D-range 2;
- monitor channel change inputs from D-range 2;
- generate timing waveforms for CTCSS detection;
- coordinate and implement timing control of the receiver;
- control the front panel "Supply" LED (refer to Section 5.3).

2.10 Synthesised Local Oscillator

(Refer to the synthesiser circuit diagram (sheet 7) in Section 6.3 and the VCO circuit diagram in Part E.)

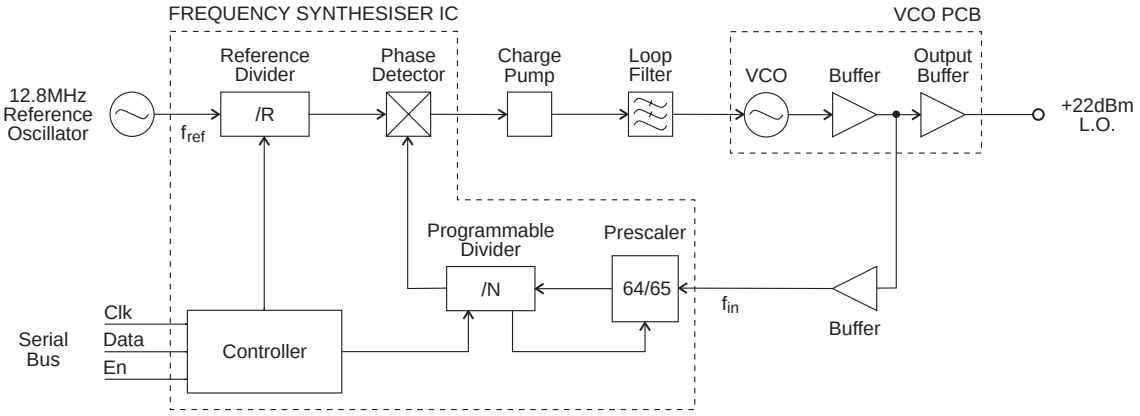

Figure 2.6 T855 Synthesiser Block Diagram

The synthesiser (IC740) employs a phase-locked loop (PLL) to lock a voltage controlled oscillator (VCO) to a given reference frequency. The synthesiser receives the divider information from the control microprocessor via a 3-wire serial bus (clock, data, enable). When the data has been latched in, the synthesiser processes the incoming signals from the VCO buffer (f_{in}) and the reference oscillator (f_{ref}).

A reference oscillator at 12.8MHz (IC700) is buffered (IC710) and divided down to 6.25kHz or 5kHz within the synthesiser IC (IC740).

A buffered output of the VCO is divided with a prescaler and programmable divider which is incorporated into the synthesiser chip (IC740). This signal is compared with the reference signal at the phase detector (also part of the synthesiser chip). The phase detector outputs drive a balanced charge pump circuit (Q760, Q770, Q775, Q780, Q785) and active loop filter (IC750, Q790) which produces a DC voltage between 0V and 20V to tune the VCO. This VCO control line is further filtered to attenuate noise and other spurious signals. Note that the VCO frequency increases with increasing control voltage.

2.11 VCO

(Refer to the VCO circuit diagram in Part E.)

The VCO transistor (Q1) operates in a common emitter, and uses a transmission line resonator (TL1). The transmission line is used in a two port configuration with varicaps positioned at one end. The VCO control voltage from the loop filter (IC750) is applied to the varicaps (D1 & D2) to facilitate tuning. The VCO output is coupled into a cascode amplifier stage (Q2 & Q3) which supplies +10dBm (nominal) output. Further amplification in Q5 brings the output drive level to +20dBm to drive the mixer.

A low level "sniff" is taken from the input to Q5 to drive the divider buffer to the synthesiser (IC740).

The VCO operates at the actual frequency required by the first mixer, i.e. there are no multiplier stages.

The VCO frequency spans from either 355-395MHz, 395-435MHz or 435-485MHz according to product type (refer to Section 1.4). The VCO is tuned to 45MHz below the desired receive frequency (low side injection) to produce a 45MHz IF signal at the output of the mixer.

2.12 Received Signal Strength Indicator (RSSI)

(Refer to the T800-04-0000 RSSI PCB circuit diagram in Section 6.2 and the IF section circuit diagram (sheet 3) in Section 6.3.)

The RSSI option PCB plugs directly into the main PCB (support circuitry being fitted as standard). It is fitted to the T855 whenever receiver signal strength monitoring is required, e.g. trunking or voting. Its function is to provide a DC voltage proportional to the signal level at the receiver input. The DC voltage is available at D-range 1 (PL100 pin 5).

The RSSI also provides the capability for high level signal strength muting, which may be selected on PL250 (refer to Section 3.5). The mute threshold may be set between -115dBm and -70dBm by RV235.

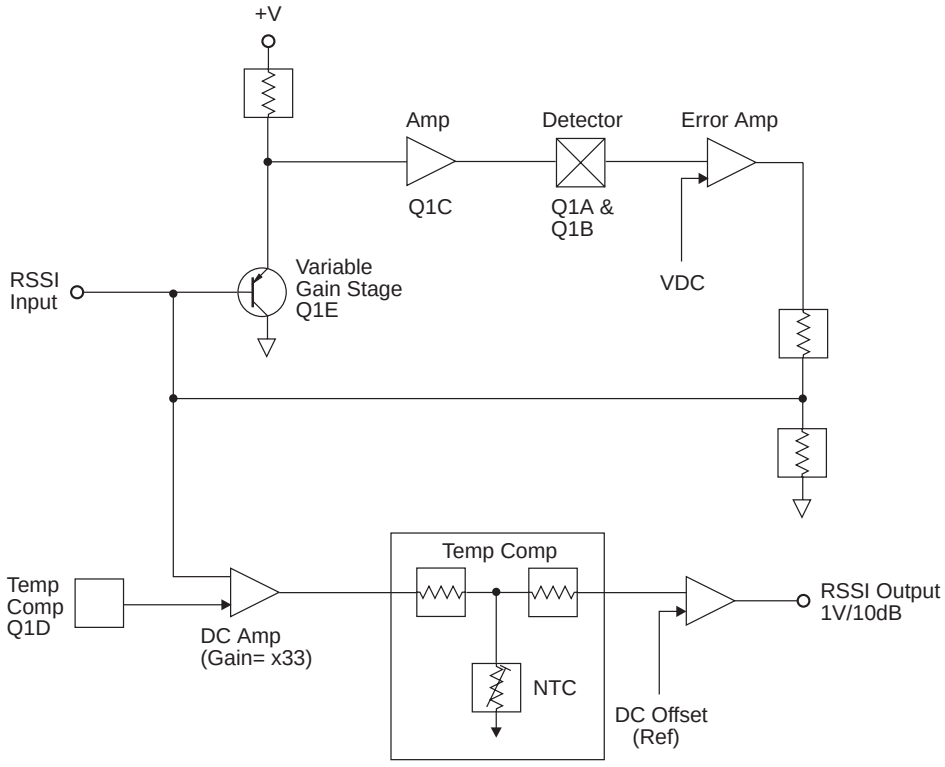

Figure 2.7 T855 RSSI Block Diagram (T800-04-0000 RSSI PCB)

The variable gain stage (Q1A) is a common emitter amplifier with its emitter grounded and the AGC control loop voltage applied to its base. Since the AGC loop will maintain a constant signal level at the collector, the gain of Q1 must be proportional to the incoming 455kHz signal level. The gain of Q1 is linearly proportional to its collector current which itself is exponentially related to the base-emitter voltage. Thus there is a logarithmic relationship between the base-emitter voltage and the gain. The circuit therefore produces a feedback voltage, and an output voltage, logarithmically related to the RF input signal.

The AGC loop is followed by a DC amplifier which provides level shifting, temperature compensation and gain to give a nominal 1V/10dB at the RSSI output. RV320 on the main PCB is used to set the RSSI voltage to a fixed value at a given RF input signal strength.

